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Ashok K.Sharma, Logic Handbook: PLDs, CPLDs, and FPGAs by Ashok K

Patent us7112994 - three dimensional integrated

load PMOS based SRAM cells can be used for PLDs and FPGAs. fabricate a generic field programmable gate
Ashok K. Sharma, "Programmable Logic Handbook

Management considerations for in-system

revolutionized the world of programmable logic by programmable PLDs with well over 90% market share, CPLDs (ispLSI 3448), all

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Reference; 1: Ashok K. Sharma, "Programmable Logic Handbook

Patent us7795913 - programmable latch based

Ashok K. Sharma, "Programmable Logic Handbook-PLDs Logic Handbook PLDs, CPLDs, & FPGAs",
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"Programmable logic handbook PLDs,

Patent us7064018 - methods for fabricating three

A generic field programmable gate array This technology provides a frame work for modular
substitution to make PLDs for Ashok K. Sharma, "Programmable Logic

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Us7812458 - pad invariant fpga and asic

Field programmable gate array core Ashok K. Sharma, "Programmable Logic Handbook-PLDs Ashok K. Sharma, "Programmable Logic Handbook PLDs, CPLDs, & FPGAs

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Patente us7795913 - programmable latch based

The latch can be used in a generic field programmable Ashok K. Sharma, "Programmable Logic Handbook-PLDs Programmable Logic Handbook PLDs, CPLDs

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Patent us7285982 - configuration circuits for

(PLD) or Field Programmable Gate Array Ashok K. Sharma, "Programmable Logic Handbook-PLDs, CPLDs Dessa data tillhandah lls av IFI CLAIMS Patent

Patente us8499269 - timing exact design

A device having a design conversion from a field programmable Ashok K. Sharma, "Programmable Logic K. Sharma, "Programmable Logic Handbook-PLDs

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Definitions and Basic Properties Robert Technology mapping issues for an FPGA with lookup tables and PLA K.: Programmable Logic Handbook, PLDs, CPLDs,

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Simple programmable logic device. Programmable Logic Devices (PLDs) * Complex Programmable Logic Devices (CPLDs) * Field Programmable Gate Arrays

Patent us7627848 - bit stream compatible fpga to

A method of converting designs from a field programmable gate array Patents Publication number Ashok K. Sharma, "Programmable Logic Handbook-PLDs, CPLDs,

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Author/Creator Sharma, Ashok K. Language English. Imprint New York : McGraw-Hill, c1998. Physical description xi, 435 p. : ill. ; 24 cm. Series McGraw-Hill handbooks.

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6 efficient technology mapping method for

6 Efficient Technology Mapping Method for PAL-Based Devices A fast partitioning method for PLA-based FPGAs. Sharma, K.: Programmable logic handbook, PLDs,

Patent us7573293 - programmable logic based

The LUT can be circuits as disclosed in commonly owned U.S. patent Field programmable gate Ashok K. Sharma, "Programmable Logic Handbook-PLDs

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